FIG. 1

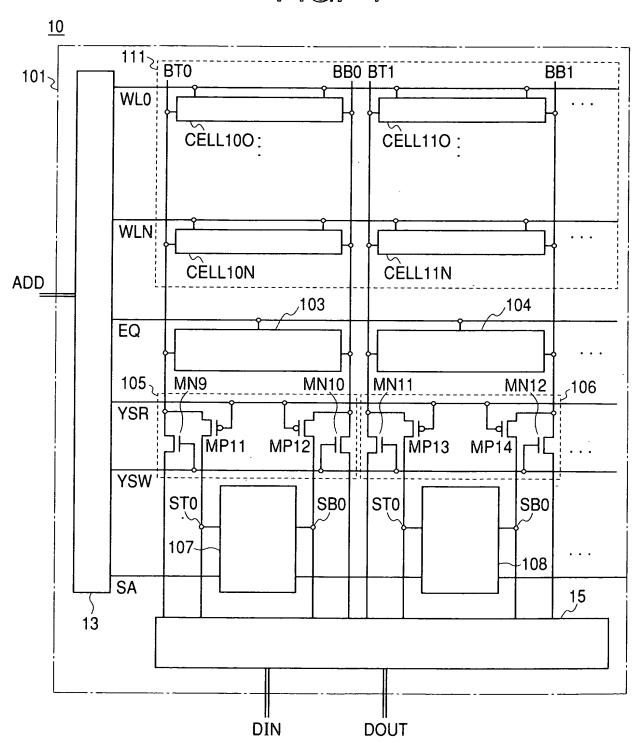


FIG. 2

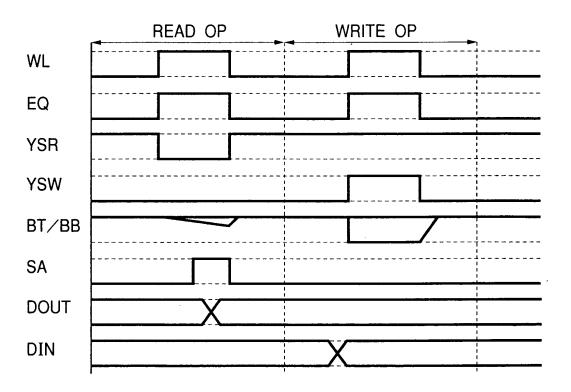


FIG. 3

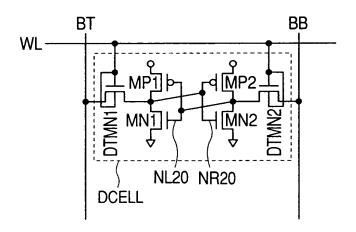


FIG. 4

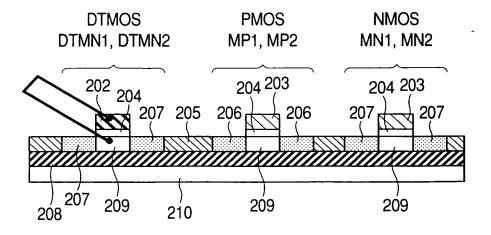


FIG. 5

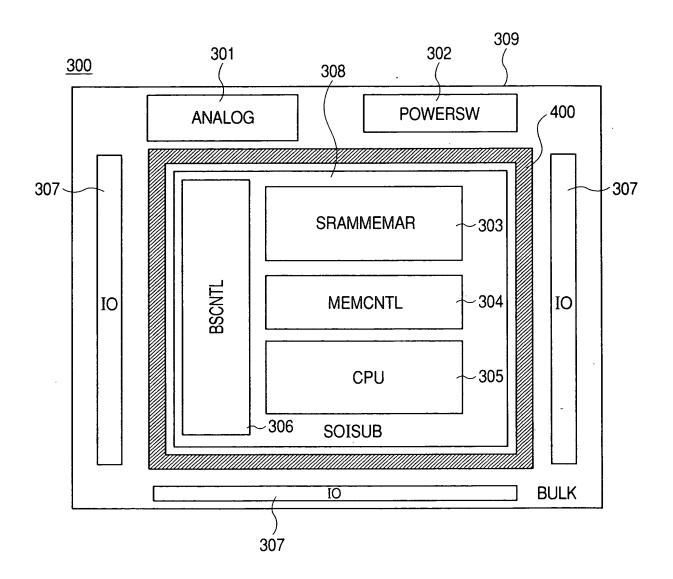
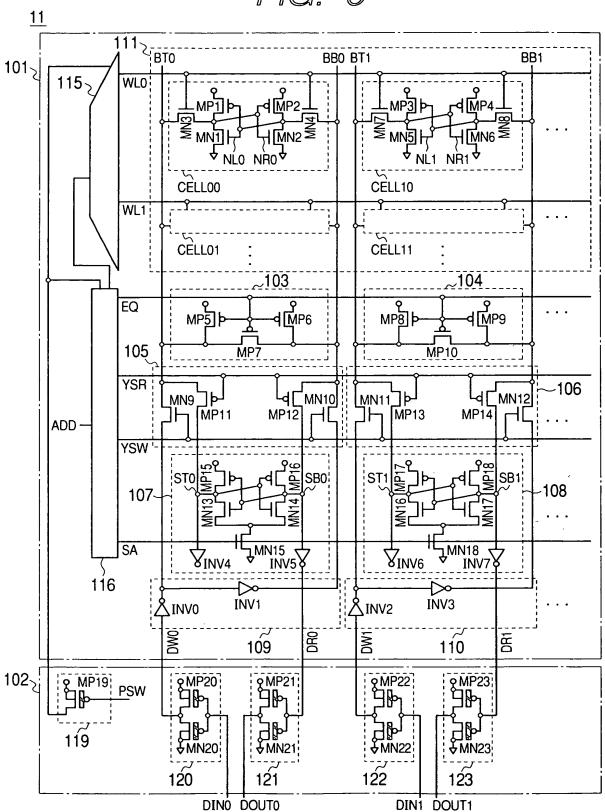


FIG. 6



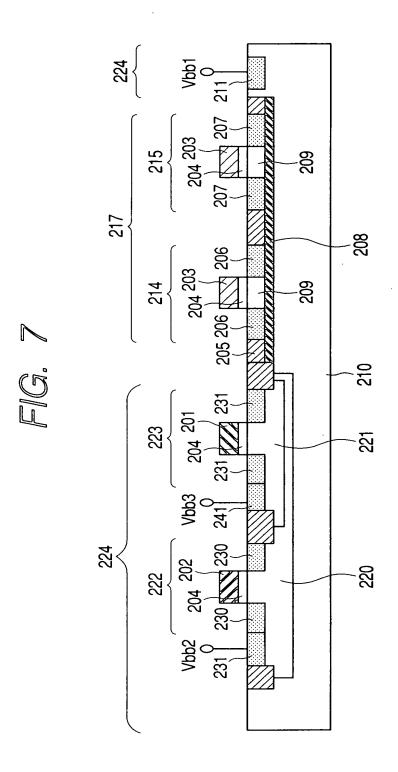


FIG. 8

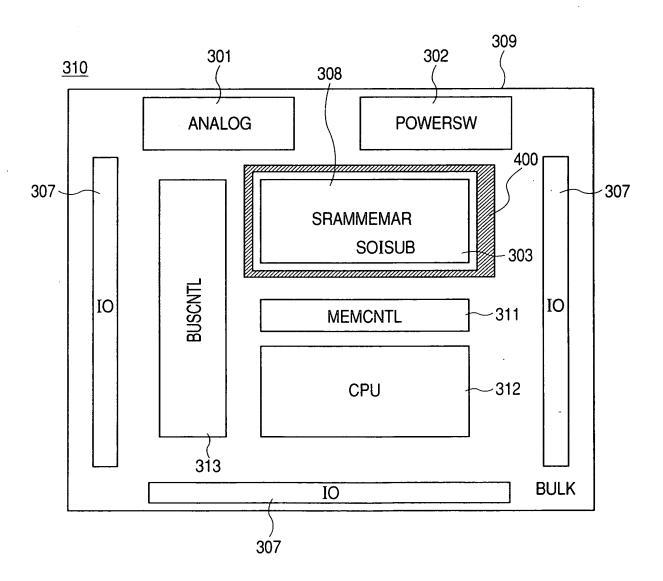


FIG. 9

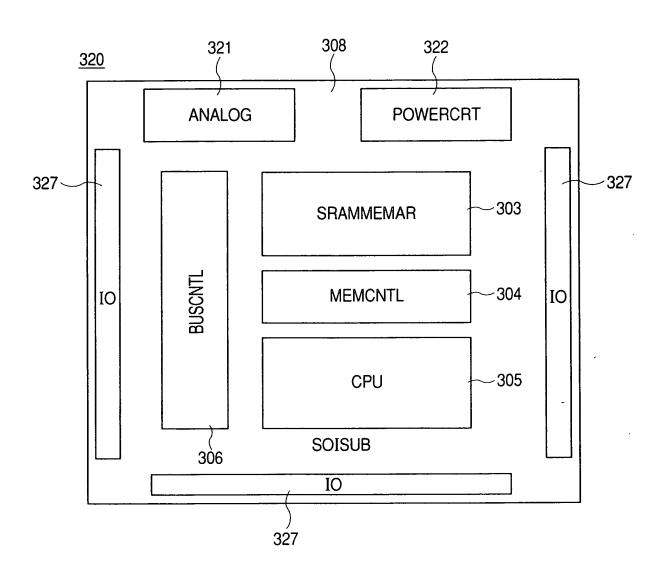
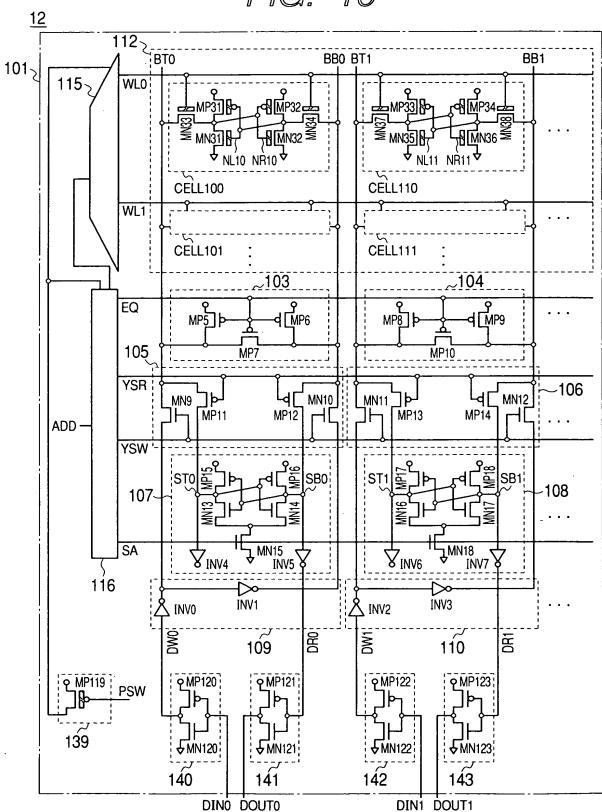
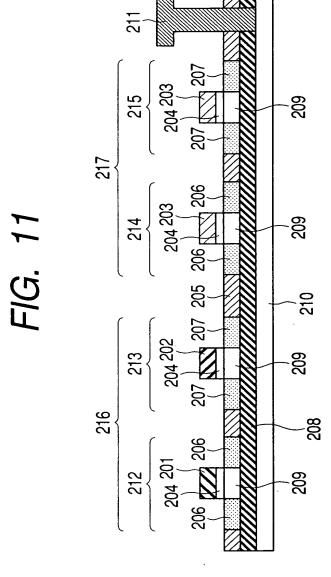


FIG. 10





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	[V]TV	-0.3	0.3	-1.0	9.0		VT[V]	-0.8	8.0	-0.8	0.8
	SOIVBB	30	38	38	30		SOIVBB	×	×	×	×
STANDARD	GATEIMP	d	d	Z	ď	LOWPOWER	GATEIMP	N	۵	Z	Ь
	GATEMAT	SiGe	SiGe	Poly-Si	Poly-Si		GATEMAT	Poly-Si	Poly-Si	Poly-Si	Poly-Si
	SUB	SOI	SOI	SOI	SOI		SUB	SOI	SOI	SOI	SOI
	VT[V]	-0.3	0.3	-0.3	0.3		VT[V]		9.0		9.0
	SOIVBB	0	0	0	0		SOIVBB	VERTICALMOS	38	VERTICALMOS	30
HIGHSPEED	GATEIMP	Ь	Ь	Ь	Ь	STANDARD	GATEIMP	VERTIC	d	VERTIC	d
	GATEMAT	SiGe	SiGe	SiGe	SiGe		GATEMAT		Poly-Si		Poly-Si
	SUB	SOI	SOI	SOI	SOI		SUB	SOI	IOS	IOS	SOI
arisios	ane	PMISFET	NMISFET	PMISFET	NMISFET	grisios	ane	PMISFET	NMISFET	PMISFET	NMISFET
S	TOP TOP	J.	רטפוני	7,400	STAIN	5	<u> </u>	-	רטפור	71400	NAM

				ביים היים					01/01/01/0		
aucoinatu		SUB	GATEMAT	GATEIMP	SOIVBB	[V]TV	BNS	GATEMAT	GATEIMP	SOIVBB	VT[V]
PMISFET	FET	SOI	SiGe	Ь	0	-0.3	IOS	SiGe	۵	38	-0.3
OGIC NMIS	IMISFET	SOI	SiGe	Ъ	0	0.3	IOS	SiGe	Ь	30	0.3
PMISFET	FET	SOI	SiGe	Ъ	0	-0.3	IOS	Poly-Si	Z	38	-1.0
NMISFET	FET	SOI	SiGe	Ь	0	0.3	IOS	Poly-Si	Ь	30	9.0
O/Analog/SW		BULK	ı	-	ı	ANY	BULK	1	ı	ı	ANY

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H D L	TERIDODE	SUB	GATEMAT	TEMAT GATEIMP	SOIVBB	VT[V]	SUB	GATEMAT	GATEMAT GATEIMP	SOIVBB	VT[V]
	PMISFET	BULK	,	ı	1	ANY	BULK	ŧ	1	-	ANY
2007	NMISFET	BULK	1	-	1	ANY	BULK	_	ı	,	ANY
	PMISFET	SOI		VERTIC	VERTICALMOS		SOI	Poly-Si	Ν	×	-0.8
OHAIN —	NMISFET	SOI	SiGe	Ь	NONE	0.5	SOI	Poly-Si	Ь	×	0.8
// Analog/SW	/SW	BULK	-	,		ANY	BULK	•	1	1	ANY

FIG. 13

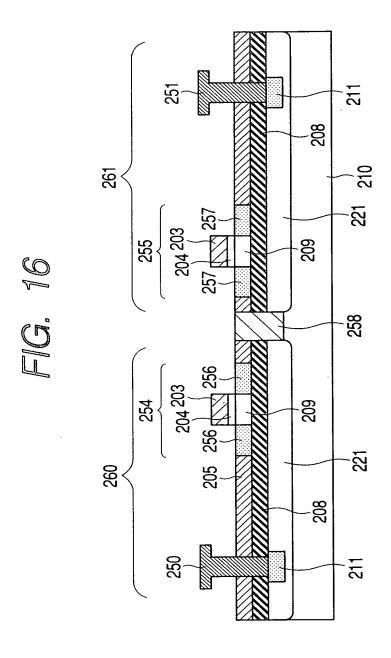
		HIGH SPEED	STANDARD	LOW POWER
		300MHz~	100MHz~300MHz	∼100MHz
i		Vdd<1.0V	Vdd≒1.0V	Vdd>1.0V
Logic	PMOSVT	-0.3V~-0.1V	-0.4V~-0.2V	-0.9V ~ -0.7V
	NMOSVT	0.1V~0.3V	0.2V~0.4V	0.7V~0.9V
SRAM	PMOSVT	-0.5V~-0.3V	-1.0V~-0.8V	-0.9V ~ -0.7V
	NMOSVT	0.2V~0.4V	0.4V~0.6V	0.7V~0.9V

FIG. 14

GATE MAT	Poly-Si		SiGe	
GATE IMP	Р	N	Р	N
PMOS Vto	+0.2V	-0.8V	-0.1V	-0.8V
NMOS Vto	+0.8V	-0.2V	0.5V	-0.2V

FIG. 15

	ELE	BULK	FD-SOI
Abbb	LVthMOS + VBBBCRT	EFFECT IS LOW UNDER 100nm	EFFECT EVEN UNDER 100nm
Vbbf	HVthMOS + VBBFCRT	EFFECT IS LOW AT HIGH TEMPERATURE LEAK CURRENT IS LARGE	HIGH TEMPERATURE OPERATION AVAILABLE, SMALL LEAK CURRENT, ON CURRENT LARGE
Vbbact	VthMOS + MNTCRT + VLTCRT	WITH ABOVE REASONS, CORRECTIONS FOR VTH DISPERSION IS NOT EFFECTIVE	EFFECTIVE UNDER 100nm & HIGH TEMPERATURE



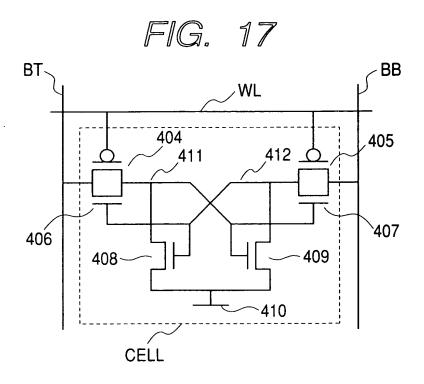


FIG. 18

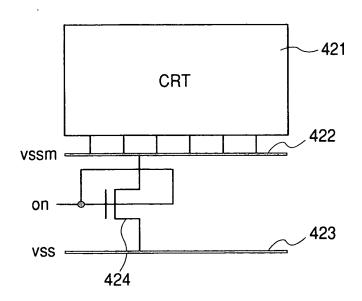


FIG. 19

